

Profile Summary: Device Engineer with extensive experience in technology support. Expertise includes SPICE modeling of FET, BJT, FLASH and volatile memories, device physics and process integration. Team player with strong analytical and communication skills and scripting abilities.

CURRENT **Innovative Silicon Inc., CA, USA.** *Member of Staff, Technology and Integration*

JUN 2008 – PRESENT **Modeling and Characterization Experience**

- Created industries first ever SPICE model to predict read/write, disturbs and retention, behavior of a floating body memory (FBM), in BSIMSOI using BJT and enhanced impact ionization models. This vital company IP was later showcased to external clients and the modeling methodology presented in a reputed modeling conference.
- Created modeling infrastructure from ground up: Interfaced with multiple vendors, finalized modeling tool for production and generated data conversion scripts for modeling. Also timely delivered SPICE models for memory cell and periphery transistors and BJTs, using BSIM4 and Gummel-Poon models.
- Devised Agilent B1500 routines, reducing cell test time by 30X over a 6 month period, significantly increasing in-house data collections capability and was given VP award for the work.
- Involved in the setup of AC retentions tests and DC Characterization of the FBM cell for MOS and BJT on Cascade S300. Also created reliability tests and routines for the memory cell.

Devices and Process Integration

- Facilitated weekly meeting with Foundry in Asia, assigned tasks to various groups, and tracked project's progress.
- Authored lot reports, correlating inline parameter to critical device metrics in dataPOWER and JMP.
- Used split analysis, DOE and TCAD to reduce operating voltage by 35% and increase retentions time up to 100X for Floating Body Memory (FBM) cell.
- Defined production tests to be run at foundry, leading to successful debug of several process and device issues including litho issues and parasitic.
- Identified leakage mechanism affecting disturbs in array operation and used process simulations in SRIM/Mastar to recommended process modification to mitigate them.
- Designed and modified test chip for cell characterization and monitoring process effects and was awarded two VP spotlight awards for timely enabling test chips.

2005-2008 **AMD, Sunnyvale, CA, USA.** *Sr. Technology and Integration Engineer*

Modeling and Characterization Experience

- Expertise in modeling leading SOI/Bulk FETs, diode, BJTs and 6T SRAM technologies (32nm, 45nm, 65nm).
- Led team project to evaluate the measurement capabilities of EAD tools for wet data and modeling median silicon behavior. Vital role in On Target Modeling (OTM) module in Agilent ICCAP.
- Responsible for $1/f$ noise models for 45nm and 65nm, and its silicon correlation. Resurrected the in-house noise measurement capabilities, saving the modeling group \$100K per year.
- Patent on noise measurement structures for accurate noise parameter extraction.

Design Support at AMD

- Handled *gm* and *rout* targets for analog modeling and improved group efficiency via portals like share point, twiki.
- Implemented a Quick Model Optimizer in PERL to rapidly generate Lot specific model libraries for product debugging, saving the group up to two weeks of modeling time for each model release.
- Provided guidance to design teams for Phase noise in PLLs and its calibration to silicon.
- Expert in DC/AC and RF characterization of single FETs and circuit.

Consolidation of Design tools across AMD

- Managed the project across California, Texas and Germany with five peer and senior members.
- Closely interacted with designers and vendors (Cadence and Synopsys) to indentify bugs (Hspice (negative rds) and Spectre (incorrect $1/f$ noise)) and make AMD specific enhancements.
- Resolved issues with DC, AC and transient simulation (Hysteresis and Ring Oscillator) consistency between Spectre and Hspice, and leveraged existing resources to finish the project before time.
- Promoted to Sr. Engineer in less than 13 months of joining AMD.

2003-2005

Lattice Semiconductors, Portland, OR, USA.

Device Engineer

Device Modeling and Design Support

- Extensive DC and AC characterization experience for FETs and Caps on various HP instruments. Generated perl script to automate benchmarking of SPICE models program, for comparison of E-test data and SPICE models.
- Created BSIM models for 90nm bulk and macro model for E-Flash cell applicable for all programming conditions.
- Generated SPICE models to predict the ESD robustness of clamps for HBM and CDM events.
- Built in house $1/f$ noise measurement setup using LNA, Spectrum Analyzer, LabView and GPIB programming

Process and Reliability

- Created foundry process splits for reducing I/O leakage and improving HBM/CDM robustness leading to better yields. Designed a test chip for ESD clamps for high speed interconnect and high voltage I/O pins.
- Patent on ESD protecting device to rectify a critical design bug. Led a team of ten design, technology and test engineers for this projects that helped in the timely launch of the PowerPac product line.
- Simulated neutron particles with iso-chromatic energies to model Soft Error Rate (SER) and optimized well profiles.

EDUCATION
2001-2003

University of California, Los Angeles. *M.S. in Solid State Electronics*

- Advisor: Dr J. Woo. Thesis, "Device Design for Sub-0.1 μ m MOSFETs for Sample and Hold Circuits", explored device designs to reduce static power consumption in sub-70nm CMOS analog circuits.
- Designed a synchronous memory bus interface in 0.25 μ m TSMC process. The controller was synthesized with Synopsys tools and the data-path was custom coded in Verilog.
- Designed a fully differential high speed high precision amplifier in Spectre, in 0.5 μ m technology using folded-cascode topology and used common mode feedback.

1997-2001

Indian Institute of Technology (IIT), Mumbai, India. *B.Tech. in Electrical Engg*

- Advisor: Dr. V.R. Rao, "RF Characterization of the Gamma Gate MOSFETs".
- Conceived and designed an audio controlled prosthetic hand for amputees. The design was taken up by government for manufacturing and has been awarded several national prizes.

SELECTED
PUBLICATIONS

- "Vertical double gate Z-RAM technology with remarkable low voltage operation for DRAM application", VLSI Symp '10
- **M. Gupta** et al, "SPICE modeling of self sustained operation to program Sub-90nm floating body cells." SISPAD '09
- "Critical current (ICRIT) based SPICE model extraction for SRAM cell", IEEE ICSICT, '08.
- S. Suryagandh, **M. Gupta**, et al, "Impact of stress on various circuit characteristics in 65nm PDSOI", ESSDERC '07
- "Analog performance of scaled bulk and SOI MOSFETs", IEEE ICSICT '04.
- **M. Gupta**, J. Woo, "Effects of gate oxide scaling and gate leakage currents on sample and hold circuits", SSDM, '04
- **M. Gupta** and J. Woo, "Device design for sub-90nm MOSFETs for sample and hold circuit", ESSDERC, '04.
- **M. Gupta** et al, "Optimization of sub-100nm gamma-gate Si-MOSFETs for RF applications", IWPSD, '01.

PROFESSIONAL
DEVELOPMENT

- Courses in statistics analysis and design of experiments via Continued Education Program at AMD
- Courses on team management and public speaking at AMD.
- Courses on Marketing, Strategy and Clean Tech Entrepreneurship at Stanford Continuing Education.

SOFTWARE
AND
EQUIPMENTS

- Programming Languages: Expert in Perl scripting and data handling, Python, MATLAB and shell programming.
- Hardware Tools: B1500, HP4140B, HP4284A, HP4155B, HP Spectrum Analyzer 3588, 200mm 300mm Cascade probe station. Prior clean room experience.
- Design Tools: PDF Solution's dataPOWER, JMP, BSIMPRO, Agilent ICCAP, Accelicon MBP, MQA, BSIM4, BSIMSOI4.0, PSP, Cadence and Synopsys tools, Sentaurus, TSUPREM4, MEDICI, Verilog, Design Analyzer, IRSIM, Sue, SRIM for SER simulation, LabView and Silicon Ensemble.

AWARDS AND
INTEREST

- 3 VP Spot light awards in 2 years at Innovative Silicon
- Founder DivvyMyRide.com, a web portal for ride sharing.
- Portland Marathon 5Miler, 25-30Yr age group award.
- Institute Special Mention for excellent performance in technical field at IIT, Bombay.
- Gold Medal, 31st All India Student Design Competition in the field of electrical engineering.
- First and Second in Institute Technology Competitions at IIT Bombay and IIT Kanpur respectively.
- Languages and Culture (Intermediate level Spanish), traveling, long distance running and investing.

References: Available on Request